REMARKS

Claims 1-8 and 18-20 are pending. Claim 1 has been amended. Claims 21-24 have been added.

I. REJECTION OF CLAIMS UNDER 35 USC §103(a)

Claims 1-8 and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim, U.S. Patent No. 6,159,778 ("Kim"), in view of Sultan et al., U.S. Patent No. 6,008,099 ("Sultan"), Vu et al., U.S. Patent No. 5,578,865 ("Vu"), and Eimori, U.S. Patent No. 5,245,208 ("Eimori"). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Kim discloses an SOI FET. The SOI FET includes an electrically insulating substrate (18/20), a semiconductor region (10) on the electrically insulating substrate (18/20), a field effect transistor (21/22/25) having a source (24a/26a), a drain (24b/26b) and a channel region (27) in the semiconductor region (10) and a metal silicide region (16) **between** the electrically insulating substrate (18/20) and the semiconductor region (10). (See, for example, the Abstract, FIG. 1, Col. 3, lines 6-40). Kim does not disclose an abrupt or hyperabrupt source/body junction, wherein the abrupt or hyperabrupt source/body junction **does not include** an implanted region similar to the implanted region at the interface between the body and the drain. Additionally, Kim does not disclose an implanted region at an interface **between the body and the drain**. Further, Kim does not disclose the implanted region providing a graded drain/body junction that is disposed at least partially under the gate. Kim also does not disclose a graded drain/body junction. Further still, Kim does not disclose a semiconductor active region disposed **directly on** the insulator layer.

Sultan discloses a method of making a lightly doped drain transistor. The method includes the steps of forming a gate electrode (52) and a gate oxide (54) over a semiconductor substrate (56) and forming a drain (70) in a drain region (58) and a source (72) in a source region (60) of the substrate (56). The method further includes generating interstitials (62) **near a lateral edge** of at least one of the drain (70) and the source (72) and thermally treating the substrate (56). The thermal treatment cause the interstitials (62) to **enhance a lateral diffusion** (84) of the drain

PAGE 5/8 * RCVD AT 2/6/2004 1:50:53 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):03-12

(70) under the gate oxide (54) **without substantially impacting a vertical diffusion** (82) of the drain (70) or the source (72). The enhanced lateral diffusion (84) **results in the formation of at least one of a lightly doped drain extension region** (75) and a lightly doped source extension region (76) without an increase in a junction depth of the drain (70) or the source (72). (See, for example, the Abstract, Col 4, lines 5-30 and FIG. 7). Sultan, like Kim, does not disclose an abrupt or hyperabrupt source/body junction, wherein the abrupt or hyperabrupt source/body junction **does not include** an implanted region similar to the implanted region at the interface between the body and the drain. Further, Sultan does not disclose an implanted region at an interface **between the body and the drain**. Further still, Sultan does not disclose the implanted region providing a graded drain/body junction that is disposed at least partially under the gate. Yet, further still, Sultan does not disclose a graded drain/body junction.

Claim 1 as amended recites the features of a semiconductor-on-insulator (SOI) device. The features include, *inter alia*, a semiconductor active region (14) disposed **directly on** the insulator layer (16). Additionally, the features include a source (30/36) and a body (34) forming an abrupt or hyperabrupt source/body junction (40). The abrupt or hyperabrupt source/body junction (40) **does not include an implanted region** similar to an implanted region (60) at the interface between the body (34) and the drain (32/36). Further, the features include a graded drain/body junction (42) **and an implanted region** (60) at an interface **between the body (34) and the drain(32/36)**, the implanted region providing a graded drain/body junction that is disposed at least partially under the gate.

Kim does not disclose an abrupt or hyperabrupt source/body junction, wherein the abrupt or hyperabrupt source/body junction **does not include an implanted region** similar to the implanted region at the interface between the body and the drain. Kim simply does not disclose an implant region at an interface between the body (27) and the drain regions (24b/26b). As the Examiner admits, Kim also does not disclose a graded drain/body junction. (page 2). Further, Kim does not disclose a semiconductor active region disposed **directly on** the insulator layer. To the contrary, Kim discloses a metal silicide region (16) **between** the electrically insulating layer (18) and the channel (27) and the source regions (24a/26a) (Col. 3, lines 23-27).

PAGE 6/8 * RCVD AT 2/6/2004 1:50:53 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):03-12

Sultan does not make up for the deficiencies of Kim. Sultan does not disclose an implanted region at an interface **between the body and the drain;** a graded drain/body junction or an abrupt or hyperabrupt source/body junction, wherein the abrupt or hyperabrupt source/body junction does not include an implanted region similar to the implanted region at the interface between the body and the drain. Sultan discloses the goal of the large tilt angle implant is **not to form a dopant profile,** but rather to generate interstitials (i.e., silicon atoms that have been knocked off their lattice sites) in the regions **near the surface** of the N-well 55. (Col. 6, lines 3-7). The interstitial regions 62 are substantially more shallow than the drain 70 and the source 72 so that the interstitials will not enhance diffusion in the vertical direction during a subsequent thermal treatment. Further, the lateral edges of the drain 70 and the source 72 substantially coincide with the lateral edge of the interstitial regions 62 so that during the subsequent thermal treatment, the interstitials enhance the lateral diffusion of the drain 70 and the source 72 under the gate oxide 54, thereby forming **a lightly doped drain extension region** 75 and **a lightly doped source extension region** 76 of the transistor 50. (Col. 6, lines 46-57). Thus, Sultan does not disclose a graded drain/body junction.

Vu and Eimori do not make up for the deficiencies of Kim and/or Sultan. That is, a device resulting from the combination of Kim, Sultan, Vu and Eimori would not include a graded drain/body junction with **an implanted region** at an interface **between the body and the drain and** an abrupt or hyperabrupt source/body junction, wherein the abrupt or hyperabrupt source/body junction **does not include the implanted region** similar to the implanted region at the interface between the body and the drain.

Therefore, claims 1-8 and 18-20 are patentable over Kim, Sultan, Vu and Eimori, either alone or in combination.

II. NEW CLAIMS

The newly added claims, i.e., claims 21-24, claim additional novel and unobvious features of the present invention. The features of claims 21-24 are supported by the specification and no new matter is believed to be added. Therefore, claims 21-24 are believed to be allowable.

PAGE 7/8 * RCVD AT 2/6/2004 1:50:53 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):03-12

Additionally, claims 21-24 depend directly or indirectly from amended claim 1. Thus, claims 21-24 are believed to be allowable for at least the reasons stated above with regard to amended claim 1.

III. CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

Any fee(s) resulting from this communication is hereby authorized to be charged to our Deposit Account No. 18-0988; Our Order No. F0541 (AMDSP0433US).

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR, LLP

Andrew Romero

Andrew Romero, Reg. No. 43,890

1621 Euclid Avenue, 19th Floor
Cleveland, Ohio 44115-2191
Telephone: (216) 621-1113
Facsimile: (216) 621-6165

R:\ARomero\Cases\AMDS\P0433US\Non-Final Reply to Office Action dated 081403 .doc

PAGE 8/8 * RCVD AT 2/6/2004 1:50:53 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):03-12